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(71) Applicant: **Hewlett-Packard Company**
3000 Hanover Street
Palo Alto,
California 94304 (US)

(72) Inventor: **Barbehenn, George**
2609 Briarwood Drive, Vancouver
Washington 98684-9153 (US)

Inventor: **Hulings, James R.**
2200 Dover Drive
Fort Collins, CO 80526 (US)
Inventor: **Badyal, Rajeev**
436 S.E. Villa
Corvallis, OR 97333 (US)
Inventor: **Allen, Ross R.**
408 Hinline Drive
Belmont
California 94002 (US)
Inventor: **Saunders, Michael B.**
4227 NW Elmwood Drive
Corvallis, OR 97339 (US)

(74) Representative: **Colgan, Stephen James et al**
CARPMAELS & RANSFORD
43 Bloomsbury Square
London WC1A 2RA (GB)

(54) **Integrated circuit printhead for an ink jet printer including an integrated identification circuit.**

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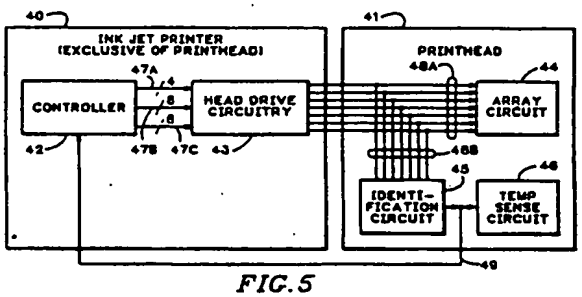

FIG. 5

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EUROPEAN SEARCH REPORT

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DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
A	US-A-4 929 969 (MORRIS) * column 3, line 60 - column 4, line 37 *	1	G06K19/07 B41J2/175
A	GB-A-2 244 339 (SAMSUNG ELECTRONICS LTD) * page 10, paragraph 1 - page 11, last paragraph; figure 4 *	1	
A	EP-A-0 389 296 (CANON KK) * column 5, line 1 - line 20 *	1	
A	WO-A-90 00971 (SIEMENS AG) * page 6, line 29 - page 7, line 10 *	1	
A	US-A-4 500 895 (BUCK ET AL) * column 1, line 56 - column 2, line 55 *	1	
A	EP-A-0 274 435 (OKI ELECTRIC INDUSTRY CO,LTD) * abstract *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	16 March 1995	Greene, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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substrate as the array circuit includes one or more programmable paths, the programmable paths corresponding and coupled to each row line. The programmable paths each include the serial combination of a programmable fuse and an active device. The opposite end of the programmable paths are coupled together at a common node, which in turn is coupled to an output circuit for providing a single serial output signal in response to a sequential polling of the row lines. The single serial output can be multiplexed onto an existing interconnect pad in order that the total number of interconnect pads on the print cartridge is not increased.

In the preferred embodiment, the identification signal is multiplexed onto an interconnection pad that is coupled to a thermal resistor divider, which provides analog printhead temperature information. The interconnect pad provides analog temperature information within a first voltage range and provides an identification signal in response to the polling of the row lines within a second voltage range.

In operation, the identification circuit provides information to the printer that reveals the type of printhead being used and, with appropriate programming, the type of manufacturing tolerances or defects in the printhead. Programming the identification circuit and polling the row lines does not adversely affect the resistor array or cause the resistor array to heat the ink reservoir and produce ink jets. The identification circuit is permanently coupled to the row lines and provides an identification output signal without increasing the number of interconnect pads on the print cartridge.

The foregoing and other objects, features and advantages of the invention will become more readily apparent from the following detailed description of a preferred embodiment of the invention which proceeds with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-2 are perspective views of an ink jet print cartridge including a flexible interconnect flex tab circuit.

FIG. 3 is a plan view of the back side of the flex tab circuit showing a metalization pattern.

FIG. 4 is a cross-sectional view of a printhead along perspective lines 4-4 of FIG. 2.

FIG. 5 is a block diagram of the ink jet printer showing the identification circuit according to the present invention and the key electrical blocks in communication with the identification.

FIG. 6 is a block diagram of the resistor array circuit.

FIG. 7 is a schematic diagram of one of the resistor cells in the array circuit.

FIG. 8 is a plot of the controller bus and drive line waveforms.

FIGS. 9-11 are schematic diagrams of three embodiments of the identification circuit of the present invention.

FIGS. 9A and 9B are schematic diagrams of pulldown and programming circuits suitable for use in the embodiment of FIG. 9.

DETAILED DESCRIPTION

Referring now to FIG. 5, the identification circuit 45 and key electrical circuits 42, 43, 44, and 46 are shown in block diagram form. In the ink jet printer 40 (exclusive of the print cartridge) a microprocessor controller 42 such as a Motorola MC 68000 sends digital data to the head drive circuitry 43 over digital busses 47A-47C. Typically, digital bus 47A is an encoded four bit address bus that contains the row addresses for selecting a row of resistor cells in the array circuit 44. Digital busses 47B and 47C are encoded eight bit "primitive" busses that contain the column addresses and timing information for selecting a particular resistor cell within a particular row of resistor cells. The number of row and column addresses handled by busses 47A-47C is related to the total number of resistors in the array circuit 44 that must be individually addressed. When decoded, the number must be equal to or greater than the total number of resistors in the array circuit 44.

In turn, the digital information carried by the digital busses 47A-47C is converted into analog pulses on drive lines 48A by the head drive circuitry 43. Only the address (row) drive lines 48A are shown in FIG. 5. The head drive circuitry 43 includes demultiplexing, level shifting, and output buffering to generate the appropriate analog pulses. The analog pulses are of sufficient duration and energy to heat the resistor cells in the array circuit 44 and boil the ink between the array circuit 44 and orifice plate 11.

The time and voltage of the pulses varies and is matched to the design of the printhead used. The waveforms for the digital busses 47A-47C and the drive lines 48A are shown in FIG. 8. The address and primitive bus waveforms are typical digital signals, switching between zero and five volts. The address bus waveform is stable for a fixed time before and after the primitive bus waveform, typically between one and seven microseconds. The row and column drive signals are typically between eight and sixteen volts, the exact voltage being dependent upon the type of resistor array circuit used.

The printhead 41 includes the resistor array circuit 44, an integrated identification circuit 45, and a temperature sense circuit 46. The analog drive

pulses are received by the resistor array circuit 44 through drive lines 48A to initiate the printing action described above. Also coupled to the address drive lines 48A are corresponding input lines 48B, which ar in turn coupled to the inputs of the identification circuit 45. The structure and operation of the identification circuit 45 is described in greater detail below. An integrated temperature sense circuit 46 is also integrated onto the same integrated circuit as the array and identification circuits 44 and 45, in order to supply temperature data to the controller 42. The output of the identification circuit 45 and the temperature sense circuit are multiplexed together, thus sharing a single, existing interconnection pad. The single output containing the identification and temperature data is supplied to the controller 42 through data output line 49.

The structure of the array circuit 44 is shown in greater detail in FIG. 6. The integrated array circuit 44 for heating the ink reservoir includes a plurality of resistor cells 39 arranged in a predetermined number of rows and columns, depending upon the desired resolution of the ink jet printer. A plurality of row lines (address lines A_0 through A_5) and column lines (primitive lines P_0 through P_5) are coupled to the integrated circuit array 44 for selecting one of the resistor cells 39. Again, the total number of row and column lines is selected for illustration purposes, only. The actual number can be more or less depending upon the application. In some cases, the number of primitive lines is seven. A resistor cell 39 is shown in greater detail in FIG. 7. Each resistor cell includes a field-effect transistor 34 for controlling current flow through the resistor 33. The resistor 33 is desirably a thin film resistor such as Tantalum Aluminum (TaAl). The resistor 33 is sized to provide sufficient thermal nergy to boil the ink in the ink reservoir. The field-effect transistor is coupled between one end of the resistor 33 and ground, with the gate being coupled to a representative row line A_N. The other end of the resistor 33 is coupled to a representative column lin P_M. Thus, current flows from the column line P_M to ground, if the corresponding row and column lines are energized.

A schematic of the first embodiment of the identification circuit 45 is shown in FIG. 9. The addr ss drive lines 48A are shown including individual drive lines A1 through A13. The number of drive lines is, of course, dependent upon the number of rows of resistor cells 39 in the array circuit 44. The exact number in FIG. 9 is for illustration only. The identification circuit 45 further includes a plurality of programmable paths corresponding and coupled to each address (row) line 48A through input lin s 48B. The programmable paths ach include the serial combination of a programmable fuse and an active d vice.

In FIG. 9, the programmable fuse is either mask programmable, a fusible link, or other type of fuse in series with the gate of a field-effect transistor. Fuses F1-F5 are typically mask programmed at the time the print cartridge 10 is manufactured. Programmable fuses F6-F13 are fabricated out of polysilicon or other suitable materials and are typically programmed by a programming circuit (seen in FIG. 9B and discussed below) after the cartridge is manufactured. The active device is a typically a field-effect transistor (Q1-Q13). The programmable path in series with the gates of transistors Q1-Q13 are programmed to make a connection to the address lines 48A to establish a digital code. The digital code generated by transistors Q1-Q13 provides information to the ink jet printer as to the type of print cartridge that is installed and other information related to manufacturing tolerances and defects. In FIG. 9, fuses F1-F5 are depicted in an undefined (either logic one or zero) logic state, and fuses F6-F13 are depicted in an unprogrammed state (either all logic one or logic zero, depending upon the convention chosen.)

The second end of the programmable paths (in FIG. 9 the second end of the programmable paths is the drain of transistors Q1-Q13) are coupled together at node 49. Node 49 forms a single output signal in response to a polling of the address lines 48A. Node 49 is a coupled to an output circuit, which is simply a pull-up resistor (not shown in FIG. 9) coupled to a positive power supply in the ink jet printer.

Figures 9A and 9B show greater detail of the identification circuit 45. In FIG. 9A, a pulldown transistor QPD1 is shown having a shorted drain and gate coupled to the gate corresponding transistor Q1. The source of transistor QPD1 is coupled to ground. While only one such pulldown transistor is shown, each transistor Q1 through Q13 includes a corresponding pulldown transistor. The pulldown transistor is necessary to pulldown the gate of transistor Q1 through Q13 if the corresponding fuse is opened. If the pulldown transistor is omitted, the gate of transistors Q1 through Q13 will float, placing the transistor, and A/D 49 node, in an indeterminate logic state.

Figure 9B shows additional circuit detail for programming fuses F6 through F13. Since fuses F6 through F13 are not mask-programmable, an additional current pulse from a programming circuit is used to program the fuse. Programming circuit 50 has an input 51 designated PROGRAM and an output coupled to the gate of transistor Q6. Programming circuit 50 includes a programming transistor QPROG6 and a pulldown transistor QPPD. Th drain of transistor QPROG6 forms the output of the programming circuit 50. The gate of transistor QPROG6 is coupled to th drain and gate of

BACKGROUND OF THE INVENTION

This invention relates generally to ink jet printers and, more particularly, to an integrated circuit for the printhead of the ink jet printer, wherein the integrated circuit contains a resistor array and an identification circuit.

Referring now to FIG. 1, shown therein is a print cartridge 10 for an ink jet printer. The print cartridge 10 contains ink reservoirs and the integrated circuit (neither are shown in FIG. 1), a printhead 12, a printhead opening or "orifice plate" 11 having a plurality of nozzles for passing a plurality of ink jets, and a flexible "tab" circuit 20 that allows for electrical connection of the printhead 12 to the ink jet printer in which the cartridge 10 is installed. Thin film resistors in the integrated circuit resistor array selectively boil ink in the ink reservoir to produce a predetermined ink jet pattern. The placement of the integrated circuit resistor array is best seen in FIG. 3 and is described below.

Referring now to FIG. 2, the printhead 12 and tab circuit 20 are shown in greater detail. The tab circuit 20 is a lead frame type of flexible ("flex") circuit that generally comprises a flexible planar dielectric substrate or film having a metalization patt rn formed on one surface thereof by, for example, sputter deposition and photolithographic etching. The back side of the flex tab circuit 20 that contains the metalization pattern is bonded to the integrated circuit in the print cartridge 10 using integrat d circuit fabrication techniques. The front side of the flex tab circuit 20 contains ground pads 25 and interconnect pads 17 for electrical connection to the ink jet printer. Also shown in FIG. 2 is further detail of the orifice plate 11, which is surrounded by insulating adhesive beads 35 for encapsulating the interconnect conductive traces to the integrated circuit in the printhead 12. The back side of the flex tab circuit 20 is shown in greater detail in FIG. 3. The metalization pattern on the back side of circuit 20 includes conductive traces 13 separated and insulated by predetermined spaces 21. The conductive traces 13 connect the integrated circuit (shown generally at 15) to the back side of the interconnect pads 17.

The printhead 12 of the print cartridge 10 is shown in greater detail in FIG. 4 along perspective lines 4-4 of FIG. 2. The simplified cross-sectional of view of FIG. 4 reveals the placement of the integrated circuit 26, which includes the thin film resistor array, in the ink reservoir 28. The ink immediat ly above the integrated circuit 26 is boiled and forced through nozzles 27, forming a pattern of ink jets.

In an ink jet printer as described above and shown in FIGS. 1-4, it is d sirable to hav several characteristics of ach print cartridge 10 easily identifiable by a controller in the printer. Ideally the data should be supplied directly by the print cartridge 10. The "identification data" provides feedback to the controller that adjusts the operation of the printer and ensures correct operation. The identified printer characteristics include, but are not limited to, ink color, architecture revision, resolution, number of nozzles 27 in the orifice plate 11, spacing between the nozzles 27, among others. In addition to the above characteristics of the print cartridge 10, it may be further desirable to characterize each print cartridge 10 during manufacturing and to supply this information to the printer. In this manner, it would be possible compensate for variations in energy supplied by the resistor array in the integrated circuit 26, ink drop volume, ink drop velocity, missing nozzles, and various other manufacturing tolerances or defects such as orifice plate 11 misalignment or non-planarity and angled orifice holes 27.

While the identification information supplied by the print cartridge 10 to the printer as described above is highly desirable, it is not desirable to add further interconnect pins 17 to the flex tab circuit 20 to carry such information. The requirements that the interconnection between the print cartridge 10 and the printer be reliable, that the print cartridge be made as small as possible, and the mechanical tolerances of the interconnect pads 17 mandate that the number of interconnect pads 17 be kept to a minimum.

Accordingly, what is desired is a method and apparatus for generating identification data directly in the print cartridge 10 to be supplied to a controller in the ink jet printer, while minimizing or even eliminating the number of additional interconnect pads 17 required to carry the identification data.

SUMMARY OF THE INVENTION

It is, therefore, a principal object of the invention to provide an identification circuit in an integrated circuit printhead of an ink jet printer while minimizing or eliminating additional interconnect pads on the print cartridge.

Another principal object of the invention is to improve the performance of an integrated circuit printhead in an ink jet printer.

According to the present invention, an integrated circuit for use in the printhead of an ink jet printer includes an array circuit for heating an ink reservoir to produce a pattern of ink jets, the array circuit including a plurality of resistor cells arranged into rows and columns. A corresponding number of row and column lines are coupled to the integrat d circuit array for selecting and energizing the resistor cells according to the desir d printing pattern. An identification circuit int grated into the sam

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(71) Applicant: Hewlett-Packard Company
3000 Hanover Street
Palo Alto, California 94304(US)

(72) Inventor: Barbehenn, George
2609 Briarwood Drive, Vancouver
Washington 98684-9153(US)
Inventor: Hulings, James R.
2200 Dover Drive
Fort Collins, CO 80526(US)
Inventor: Badyal, Rajeev
436 S.E. Villa
Corvallis, OR 97333(US)
Inventor: Allen, Ross R.
408 Hinline Drive
Belmont California 94002(US)
Inventor: Saunders, Michael B.
4227 NW Elmwood Drive
Corvallis, OR 97339(US)

(74) Representative: Colgan, Stephen James et al
CARPMAELS & RANSFORD
43 Bloomsbury Square
London WC1A 2RA (GB)

(54) Integrated circuit printhead for an ink jet printer including an integrated identification circuit.

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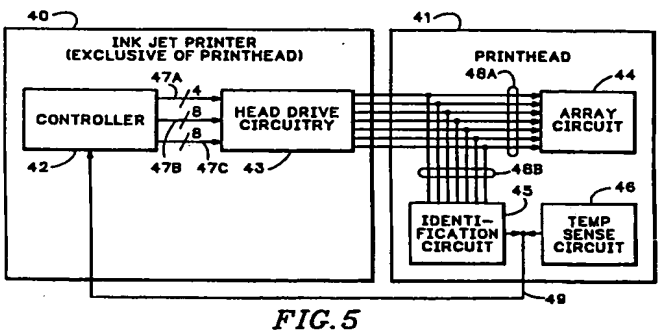

FIG. 5

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transistor QPPD to form the input 51 of programming circuit 50. The sources of both transistors are coupled to ground. Although only one programming transistor QPROG6 is shown coupled to the gate of corresponding transistor Q6, there is one programming transistor for each transistor Q6 through Q13 associated with a fuse that must be programmed with a current pulse. Thus, for the embodiment of FIG. 9, the programming circuit will have eight outputs and eight programming transistors QPROG6 through QPROG13. The gates of each of the programming transistors is coupled to the common input line 51 for receiving the PROGRAM input signal. Only one pulldown transistor QPPD, however, need be used, regardless of the number of outputs. The pulldown transistor QPPD assures that the all outputs of the programming circuit 50 are off when the PROGRAM input signal is low or an open circuit.

In operation, the programming circuit 50 is activated by supplying a logic high PROGRAM signal on input line 51. By selecting a particular address line A_N, an extra current flows through the corr sponding programming transistor sufficient to program (open) the fuse. Fuses coupled to unselected address lines remain unprogrammed (short circuited). It is important to note that, while input line 51 represents an extra input pin for the printhead, it is not necessary that input line 51 be grouped with the existing printer connector pads (best seen in FIG. 2). The extra input line connector pad can be placed anywhere on the printhead. A special programming fixture can be built to interface with the extra connector pad. It may desirable to place the programming connector pad away from the main group of printer connector pads to avoid an inadvertent entry into the programming mode.

Referring back to FIG. 9, if a programmable path is programmed to form a connection between an address line A_N and the gate of the corresponding field-effect transistor Q_N, a polling of the address line turns on the transistor and pulls node 49 low. Alternatively, if a programmable path is programmed to form an open circuit between an address line and the gate of the corresponding field-effect transistor, a polling of the address line has no effect on the turned off transistor, since the gate is pulled low, and node 49 remains high. The signal on node 49 is a serial data output corresponding to the data code formed polling the address lines coupl d to the programmable paths of the identification circuit 45.

The identification signal output at node 49 is coupled to a thermal resistor RT1, which forms a resistor divider with a pull-up resistor (not shown in FIG. 9) betw en V_{cc} and ground. The value of the thermal resistor is set to provide a suitable voltag ratio, as explained below. A typical example of desirable values for the thermal resistor and pull-up resistor are 422 ohms each. The 422 ohm value is standard for a 1% resistor, but other values can be used for each resistor, and the resistor values need not be the same. For V_{cc} equal to five volts and resistance values being equal, however, the ratio of resistor values sets a nominal voltage at node 49 of 2.5 volts. Analog information relating to the printhead temperature and digital information relating to the identification code are multiplexed together in order that an additional interconnect pad is not needed. The output signal at node 49 provides analog temperature information within a first voltage range of about two volts at 0° C to about four volts at 100° C. The same output node provides an output identification signal in response to the polling of the address lines 48A within a second voltage range. Output node 49 falls to about one volt or less when an address line A_N is polled and the corresponding programmable path has been previously programmed to form a connection to the gate of the associated transistor Q_N. The one volt signal can therefore be used as a logic zero. If the programmable path has been previously programmed to form an open circuit, the preexisting analog temperature voltage does not change. The two to four voltage temperature voltage can therefore be used as a logic one.

An alternative embodiment of the identification circuit 45 is shown in FIG. 10, wherein the active device in the programmable path is a diode. In this embodiment, the output portion of the identification circuit includes a resistor R1 and field-effect transistor Q1 coupled to the common node 49'. Resistor R1 is desirably a polysilicon resistor having a value of 1K ohms, but can be made in a manner suitable to an integrated circuit process such as NiCr resistors or self-biased FETs. A signal voltage is developed across resistor R1 in response to current flow through any of the diodes D1-D13 that are programmably coupled to the address lines. The signal voltage is in turn coupled to the gate of the transistor Q1. Transistor Q1 turns on and off in response to current flow in the programmable paths in a similar fashion to the transistors Q1-Q13 as described in the embodiment of FIG. 9. Diodes D1-D13 are necessary for current steering. A programming circuit 50 having a single programming transistor and a single pulldown transistor has an input 51 for receiving the PROGRAM input signal and a single output coupled to common node 49'.

Another alt rnative embodiment of identification circuit 45 is shown in FIG. 11. This embodiment is similar to the mbodiment of FIG. 10, except that two programmabl paths are used for each address line. For xample, a programmable path that includes diode D13 and D26 is coupled to addr ss

line A1. The embodiment of FIG. 11 is desirable if more bits are needed in the identification signal. Rather than a single output transistor, the identification circuit 45 of FIG. 11 includes transistors Q1 and Q2, the gate of which is coupled to a respective row of diodes. The drains of transistors Q1 and Q2 are coupled together to form a single output that is multiplexed with the analog temperature information at node 49. The source of transistors Q1 and Q2 are respectively coupled to the drain of transistor Q3 and Q4. Primitive signals P0 and P1 turn on either transistor Q3 or Q4, and thus enable either transistor Q1 or transistor Q2 to pass the identification signal to the output node 49. In order not to damage the resistors in the resistor array, is desirable that the pulse width of the primitive signals P0 and P1 not be extended beyond the normal pulse width. Separate programming circuits 50A and 50B are provided to program each set of transistors.

With respect to each of the embodiments shown in FIGS. 9-11, the fuses are programmed according to a predetermined pattern. Part of the pattern can be programmed at preassembly (through mask programmable fuses) to identify the print cartridge and part of the pattern can be programmed after the print cartridge is assembled (through integrated current programmable fuses) to provide compensation information to the controller. Programming the fuses includes the step of forming an open-circuit path between an address line and an active device in response to a logic high signal impressed on the selected address line and a current pulse from a programming circuit. A short-circuit path remains coupled to the unselected address lines.

Once the predetermined pattern of short and open circuit paths is programmed into the identification circuit, each row line can be polled to ascertain the identification data. If the primitive connections to the resistor array circuit are disconnected or the primitive voltage pulses are not used, no power is consumed in the resistor array and the address polling pulses can be as long as desired. Otherwise, short address polling pulses are desirably used that are not of sufficient duration to cause significant heating in the resistor array. The polling of the row lines causes a signal current to flow through the programmable paths that are programmed in a first logic state (short circuit) and no curr nt to flow through the programmable paths that ar programmed in a second logic state (open circuit). The signal currents of the programmable paths are combined to form a single serial output identification signal. If desired, the output identification signal can be multiplexed onto an existing interconnection pad of the printhead, such as the thermal resistor divid r circuit described above.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it is apparent to those skilled in the art that the invention can be modified in arrangement and detail without departing from such principles. For example, while certain types of materials and component values have been specified, it is apparent to those skilled in the art that other types of suitable materials and component values may be used, depending upon the application requirements. Also, while a certain number of address lines and programmable paths have been shown, any number may be used. The ratio of mask programmable fuses to current programmable fuses can also be changed. The fuses may be integrated onto the array circuit 44 or imbedded in the flex circuitry, if desired. While a specific programming circuit has been shown, other such programming circuits are possible to provide the additional current programming pulse. The programming circuit may be eliminated entirely, and non-current programmed fuses such as laser ablated fuses may be used. Also, fuses may be omitted during the fabrication process and connections created or grown as needed. We therefore claim all modifications and variation coming within the spirit and scope of the following claims.

Claims

1. An integrated circuit for use in a printhead comprising:

   an array circuit (44) for heating an ink reservoir to produce a pattern of ink jets, the array circuit including a plurality of resistor cells (39) arranged in a predetermined number of rows and columns;

   a plurality of row and column lines coupled to the integrated circuit array for selecting at least one of the resistor cells; and

   an identification circuit (45) including a plurality of programmable paths, at least one of the paths corresponding and coupled to each row line.

2. A circuit as in claim 1 in which a first end of the programmable paths are coupled to the respective row line and a second end of the programmable paths are coupled together at a common node.

3. A circuit as in claim 2 in which the identification circuit furth r compris s an output means having an input coupled to the common node and an output for providing an output signal in response to a polling of the row lines.

4. A circuit as in claim 3 in which the output means comprises:

a resistor (R1) coupled to the common node; and

a transistor (Q1) having a control node coupled to the common node and a controlled node forming the output.

5. A circuit as in claim 3 in which the output is coupled to a thermal resistor divider, wherein

the output provides circuit temperature information within a first voltage range and

the output provides an output signal in response to the polling of the address lines within a second voltage range.

6. A circuit as in claim 1 in which the programmable paths each comprise the serial combination of a programmable fuse and an active device.

7. A circuit as in claim 6 in which the programmable fuse comprises a fusible polysilicon link.

8. A circuit as in claim 6 in which the active device comprises a diode.

9. A circuit as in claim 6 in which the active device comprises a field-effect transistor.

10. A circuit as in claim 1 in which the resistor cells further comprise a field-effect transistor for controlling current flow through the resistor.

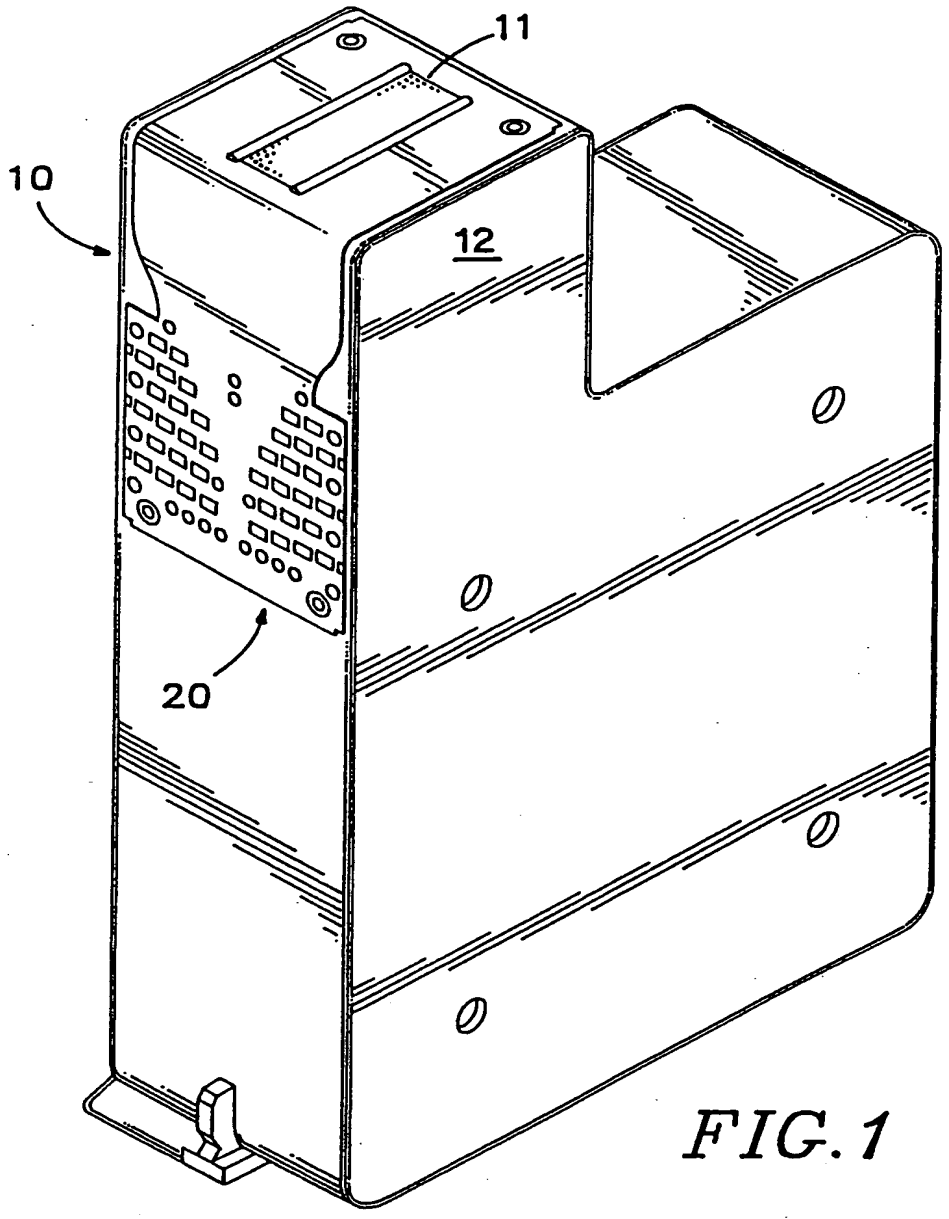

FIG. 1

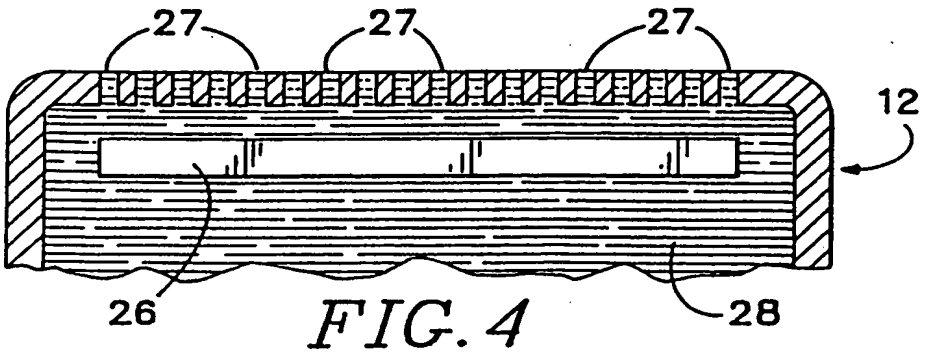

FIG. 4

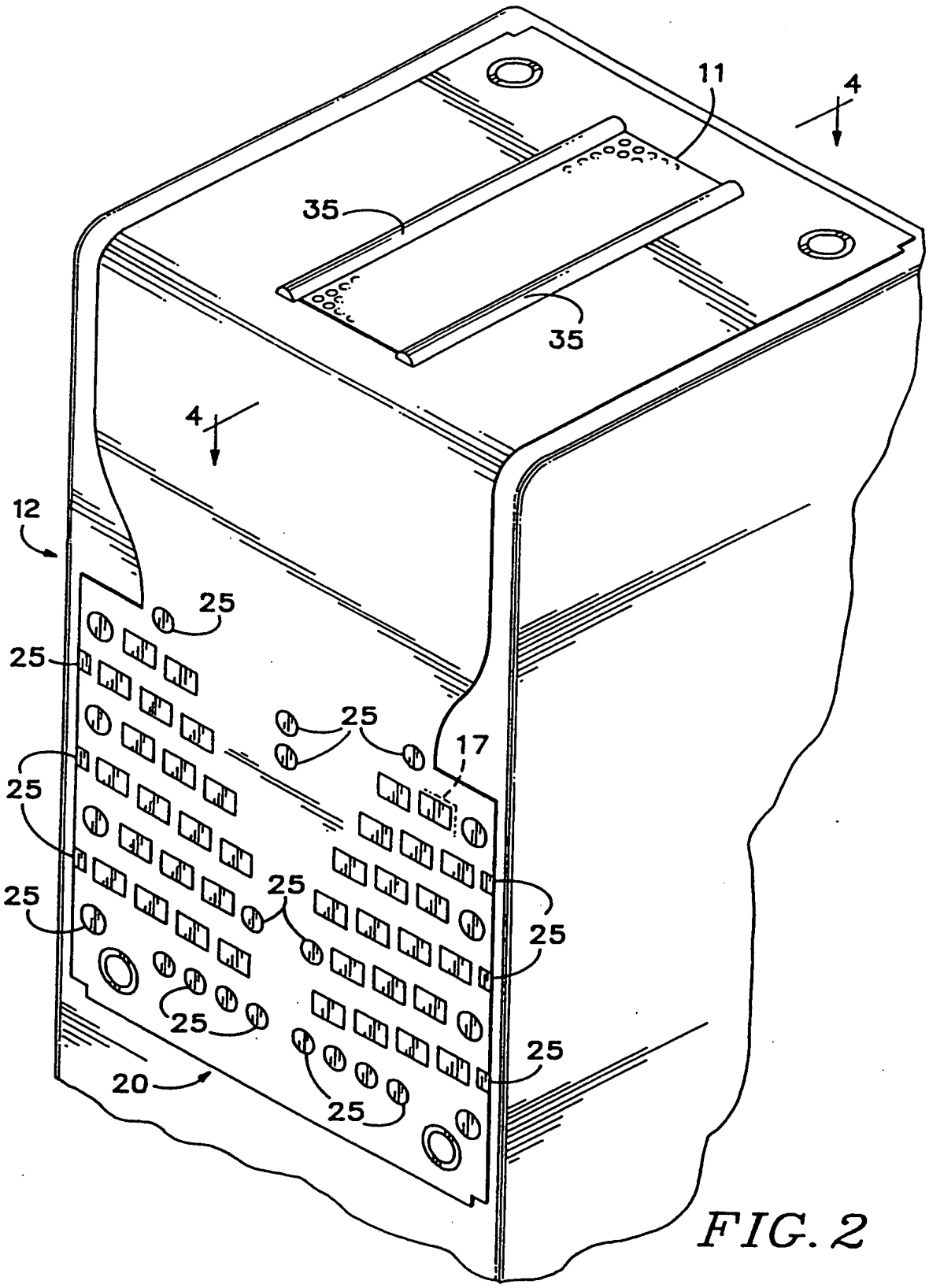

FIG. 2

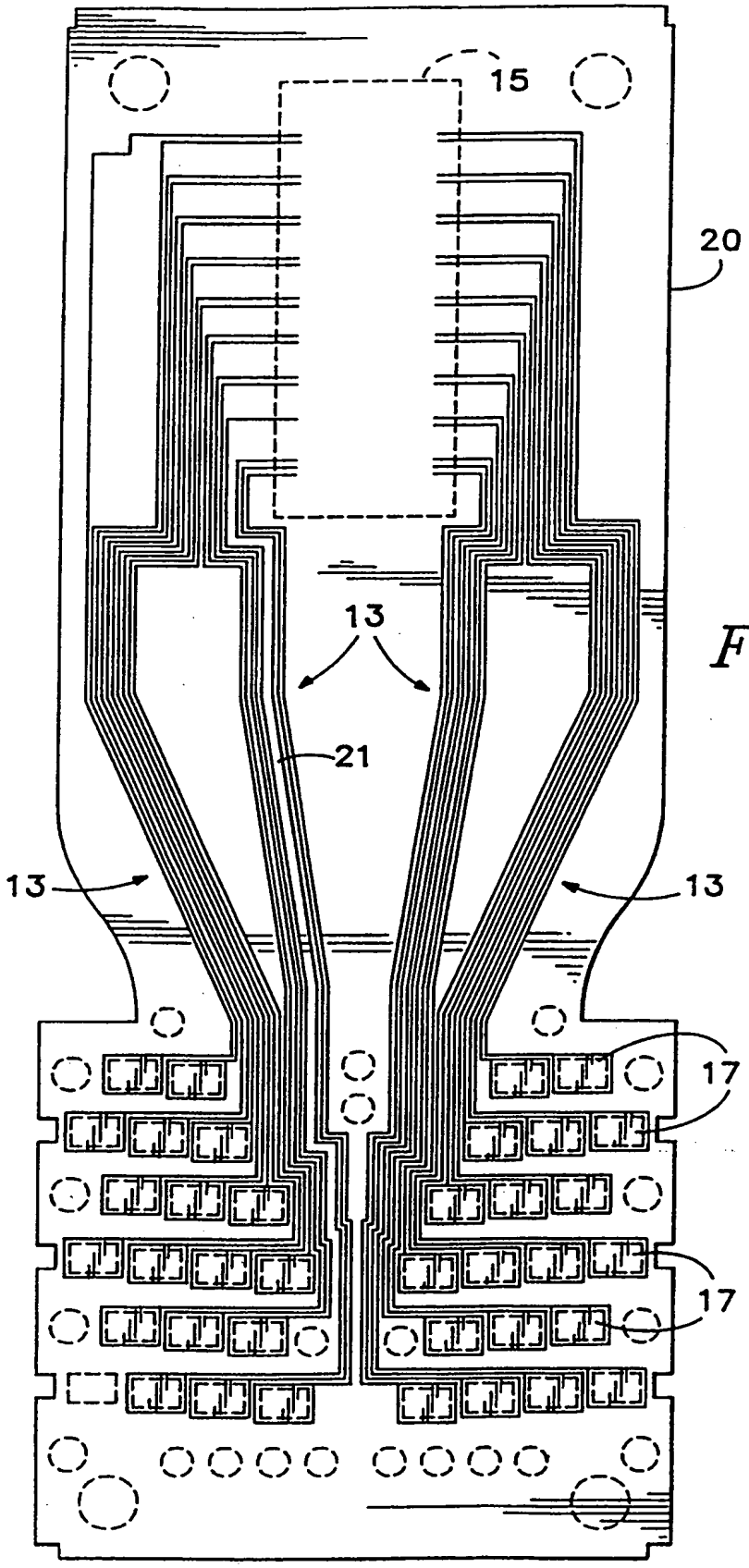

FIG. 3

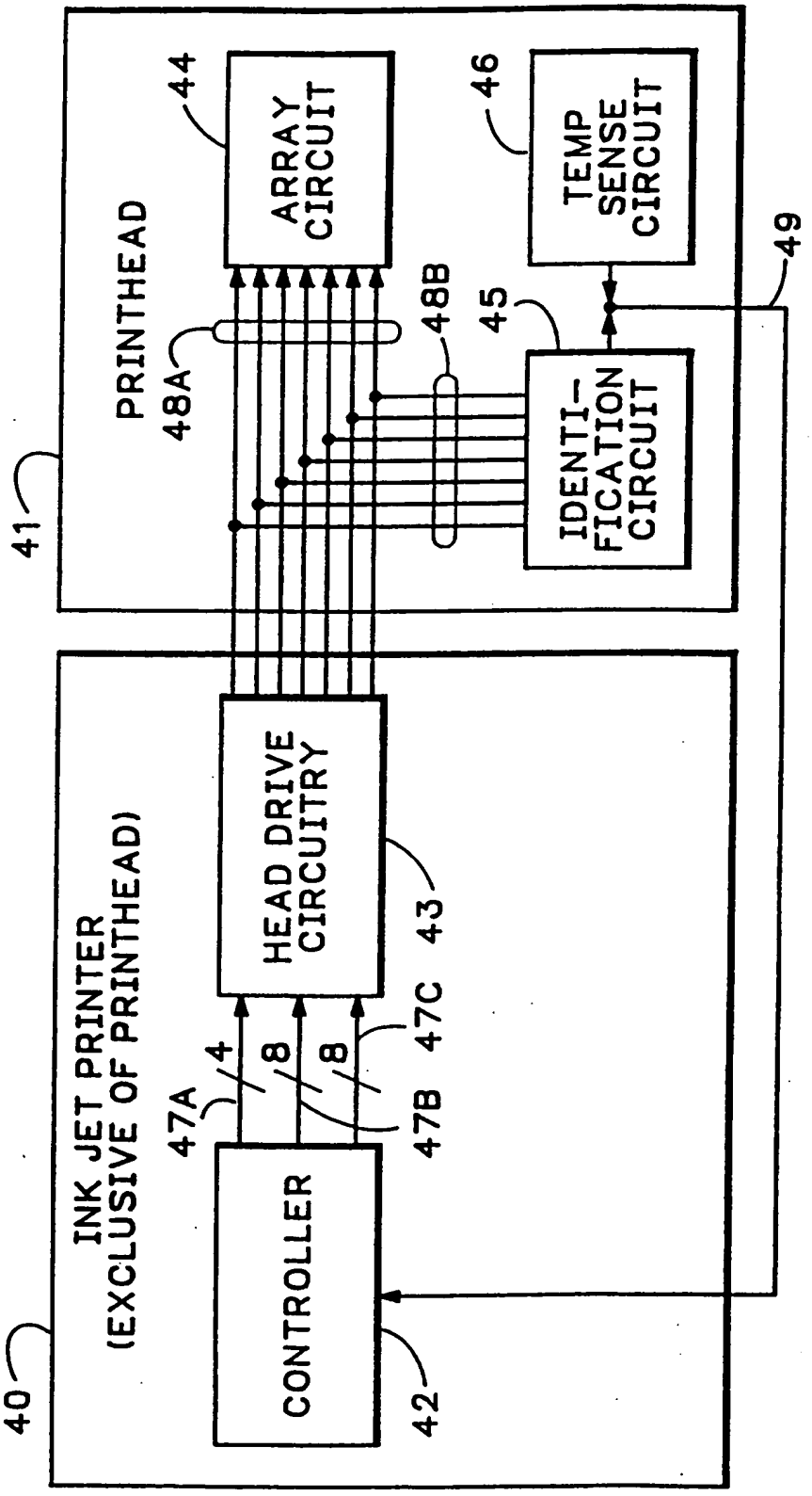
INK JET PRINTER
(EXCLUSIVE OF PRINTHEAD)
40
CONTROLLER
42
HEAD DRIVE
CIRCUITRY
43
47A
47B
47C
4
8
8
PRINTHEAD
41
48A
48B
ARRAY
CIRCUIT
44
IDENTI-
FICATION
CIRCUIT
45
TEMP
SENSE
CIRCUIT
46
49

FIG. 5

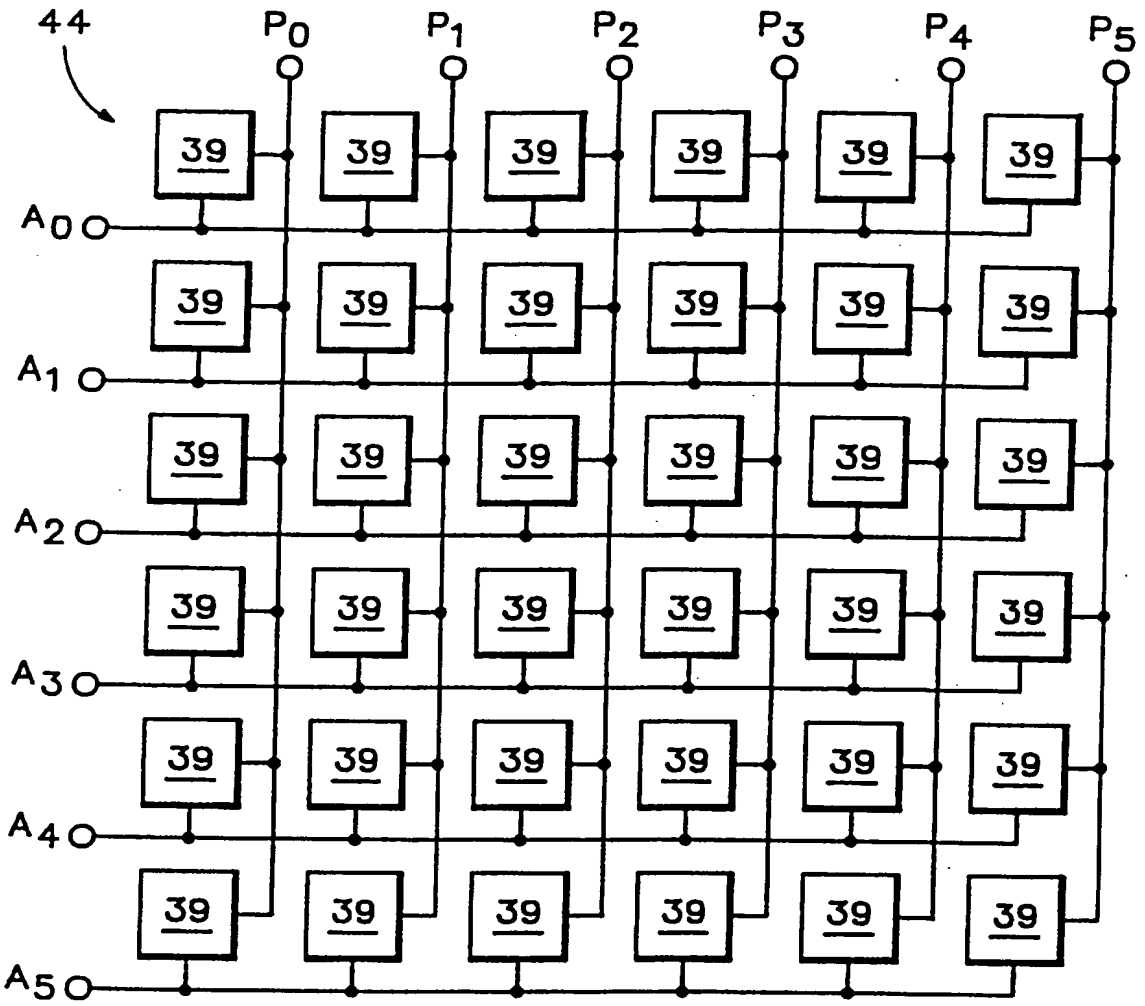

FIG. 6

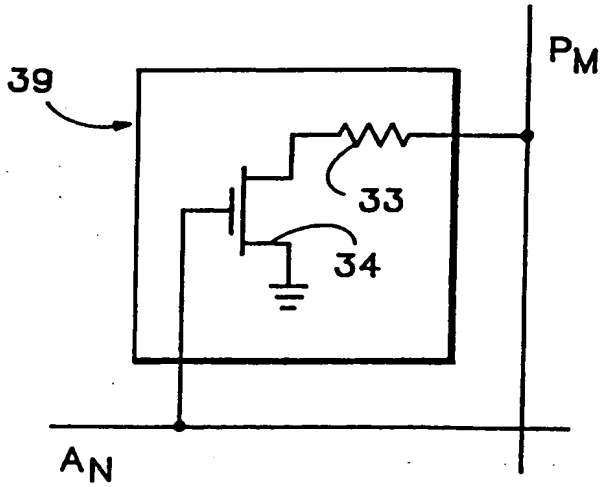

FIG. 7

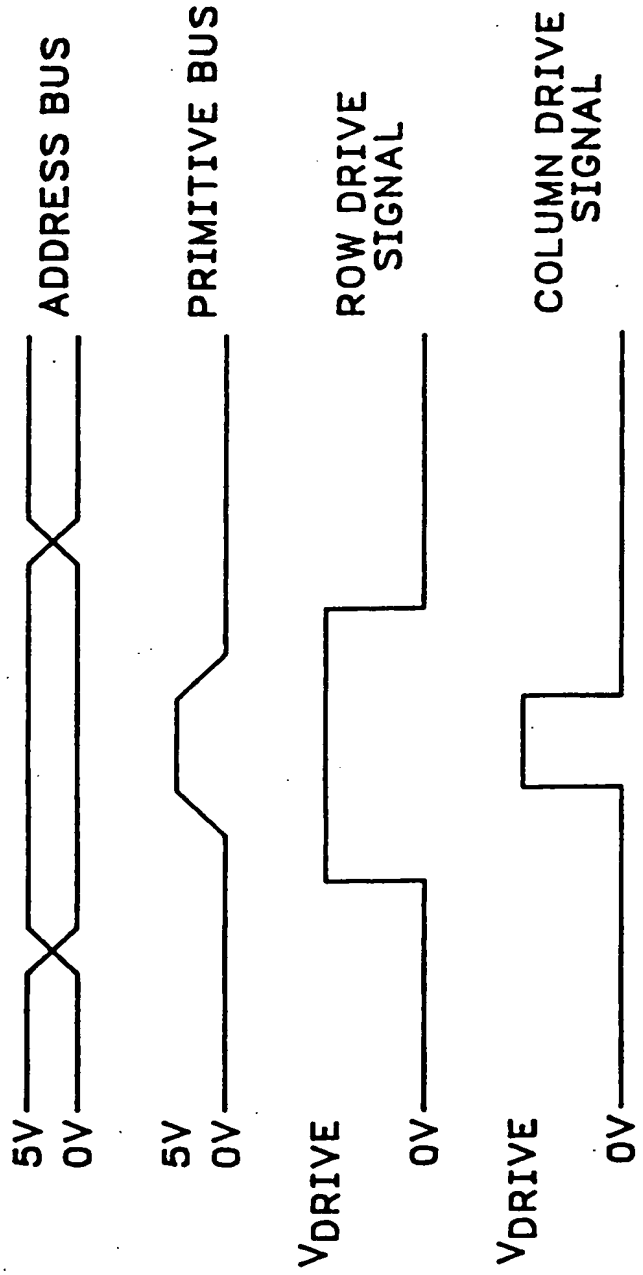
ADDRESS BUS
5V
0V
PRIMITIVE BUS
5V
0V
ROW DRIVE SIGNAL
VDRIVE
0V
COLUMN DRIVE SIGNAL
VDRIVE
0V

FIG. 8

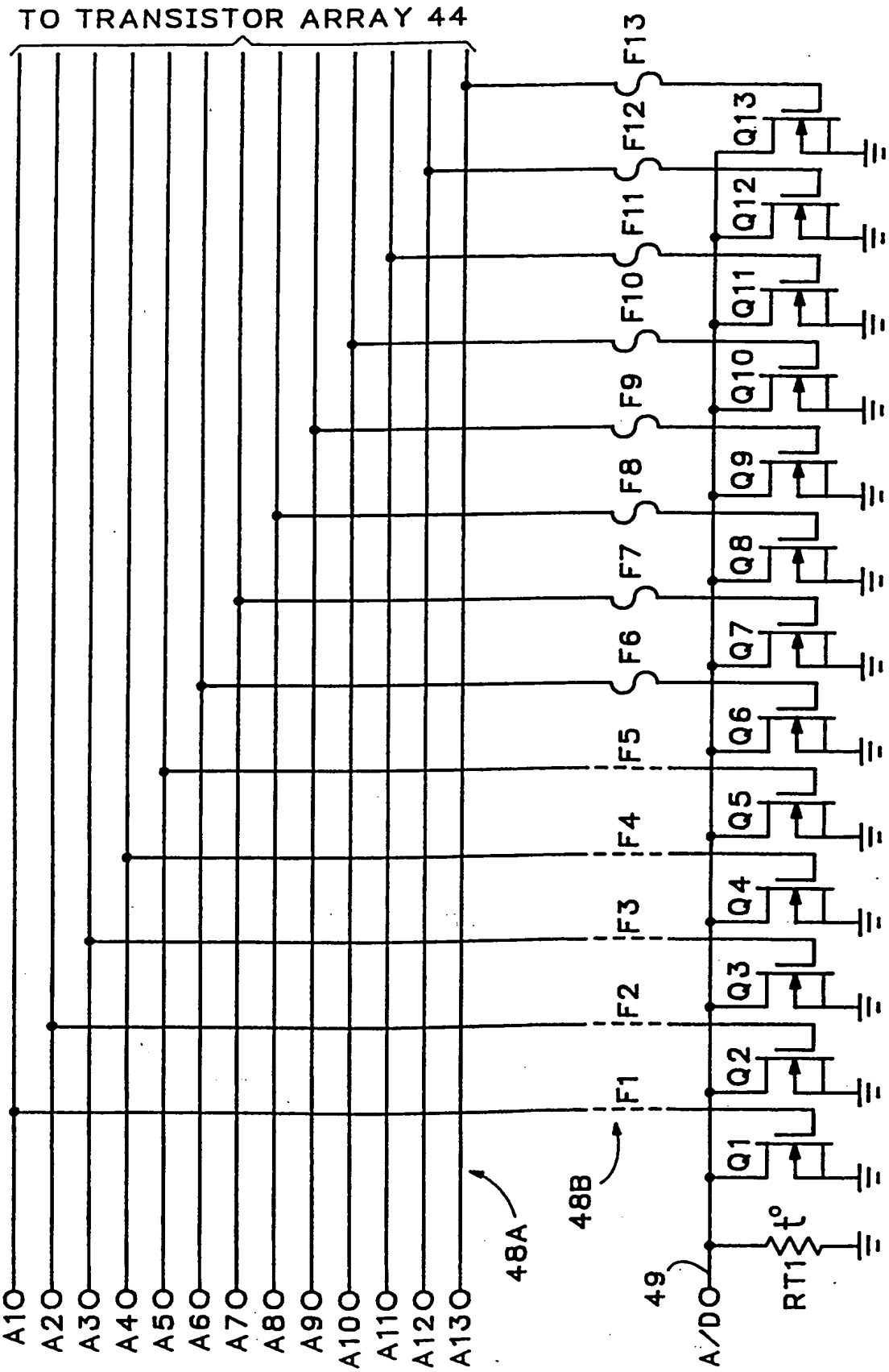
TO TRANSISTOR ARRAY 44
A1O
A2O
A3O
A4O
A5O
A6O
A7O
A8O
A9O
A10O
A11O
A12O
A13O
48A
48B
49
A/DO
RT1
t°
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F13

FIG. 9

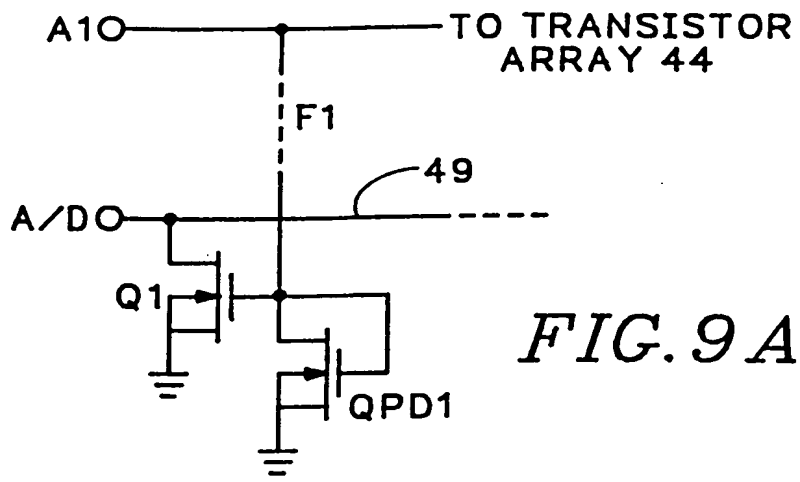
A1O
TO TRANSISTOR ARRAY 44
F1
49
A/DO
Q1
QPD1

FIG. 9A

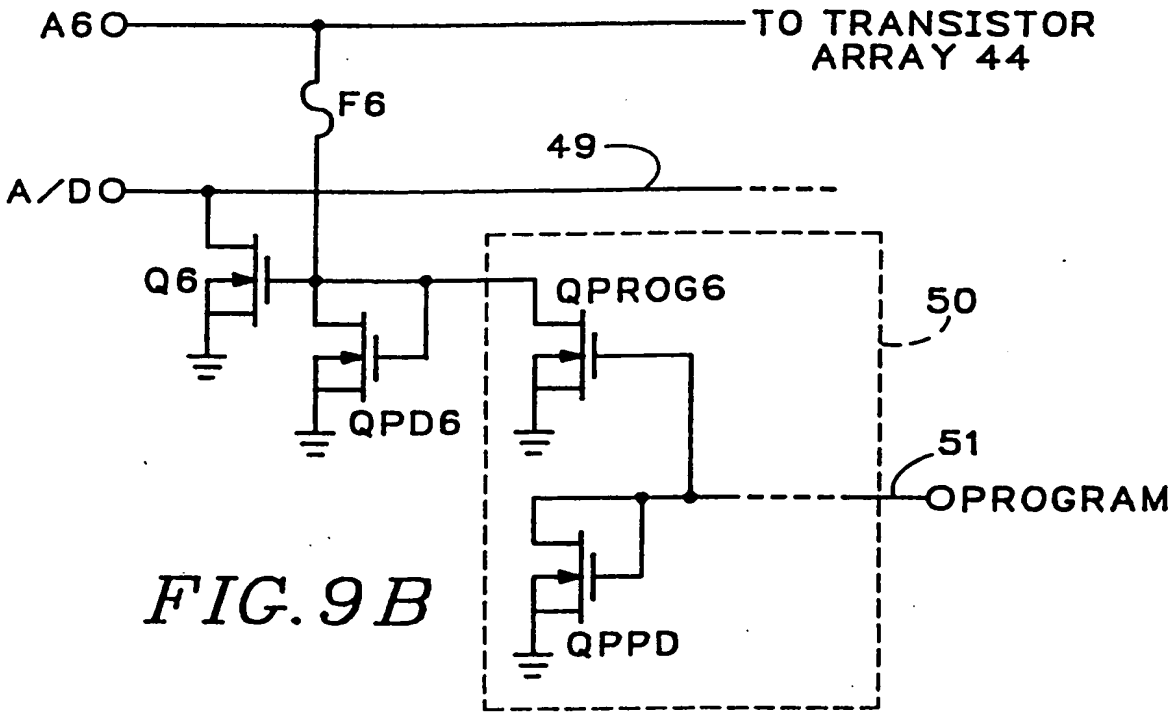
A6O
TO TRANSISTOR ARRAY 44
F6
49
A/DO
Q6
QPROG6
50
QPD6
51
OPROGRAM
QPPD

FIG. 9B

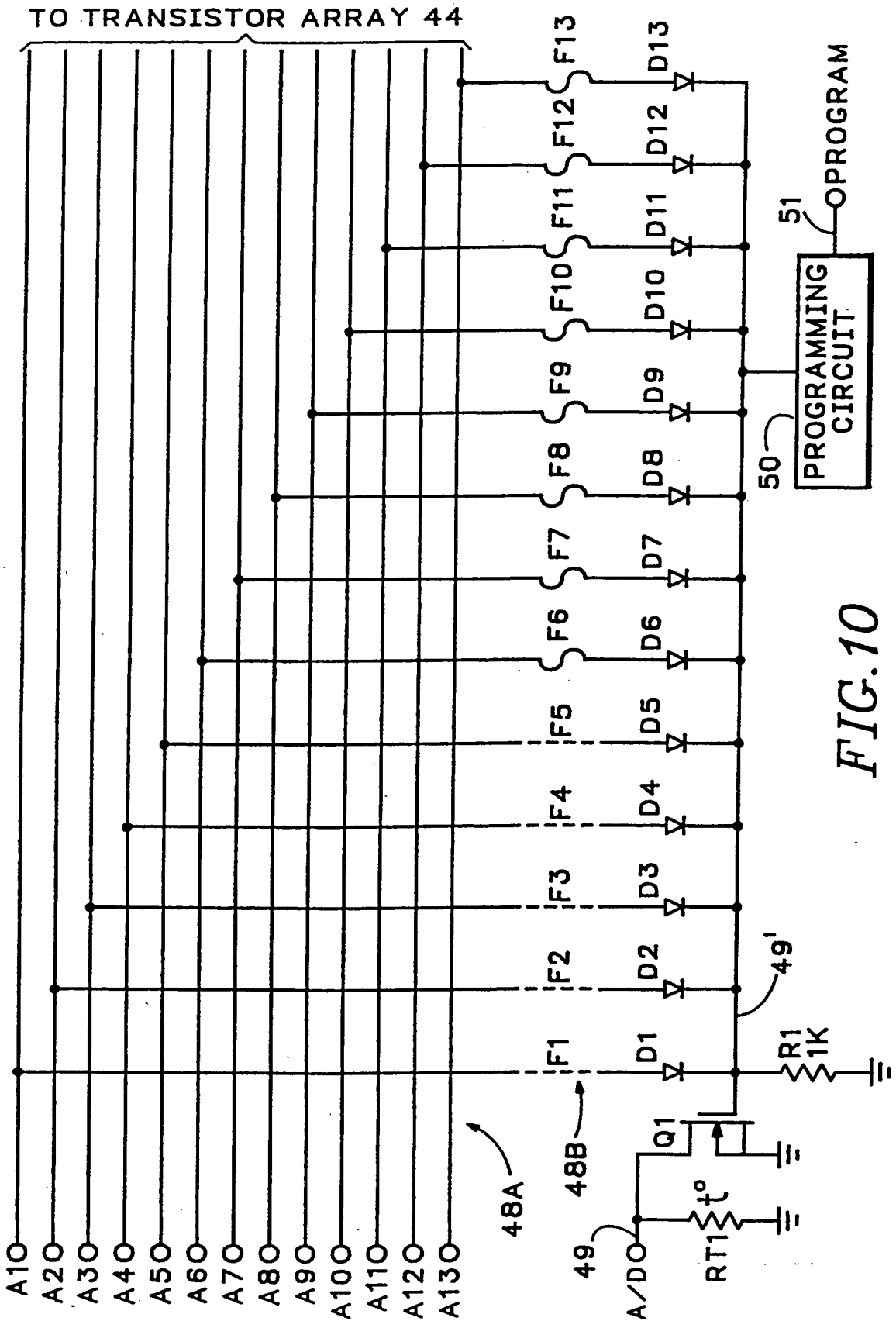
TO TRANSISTOR ARRAY 44
A10
A20
A30
A40
A50
A60
A70
A80
A90
A100
A110
A120
A130
48A
48B
49
A/D0
49'
R1
1K
RT1
t°
Q1
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F13
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
50
PROGRAMMING CIRCUIT
51
OPROGRAM

FIG. 10

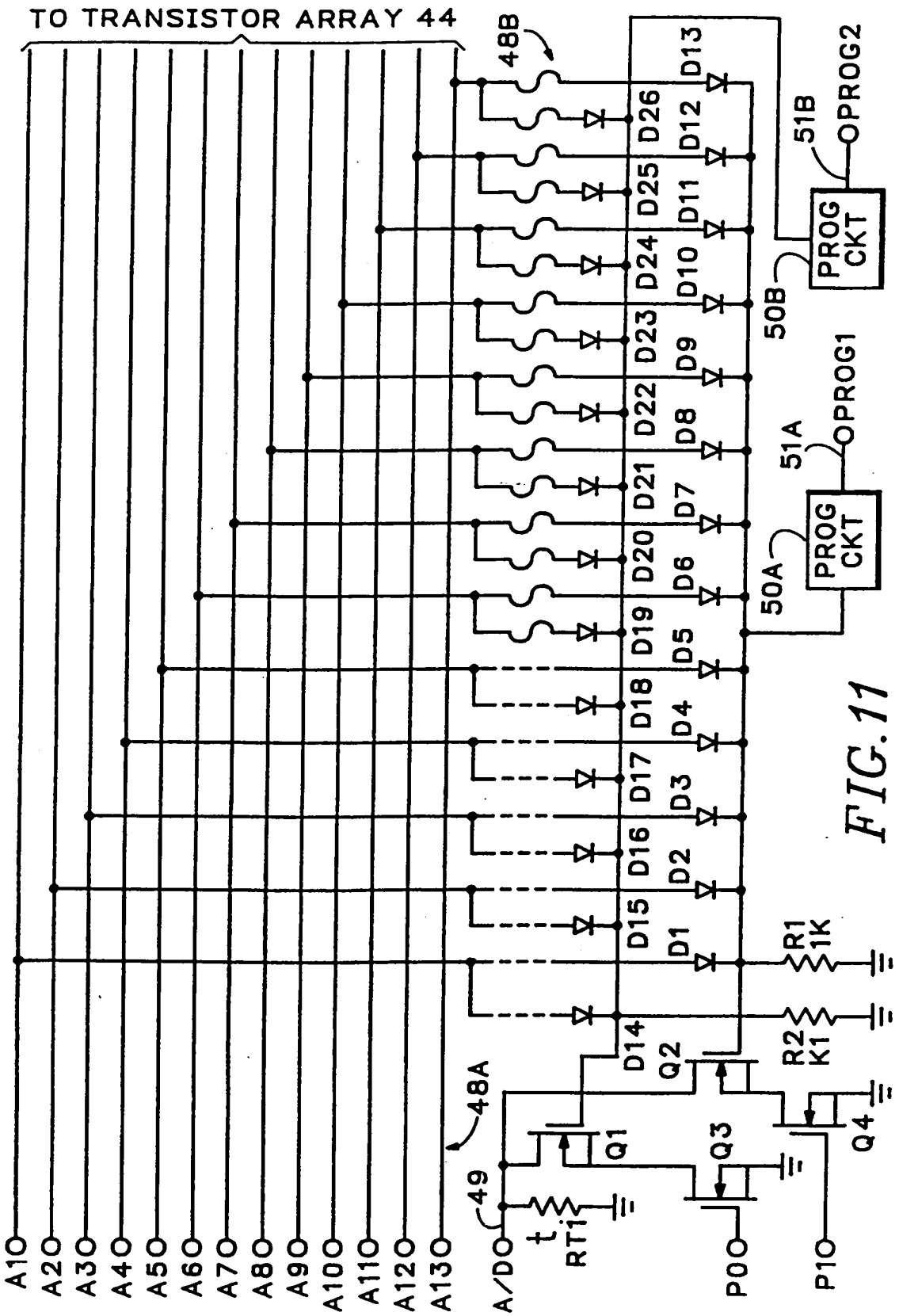
TO TRANSISTOR ARRAY 44
48B
48A
49
A1O
A2O
A3O
A4O
A5O
A6O
A7O
A8O
A9O
A10O
A11O
A12O
A13O
A/DO
RT1
Q1
Q2
Q3
Q4
P0O
P1O
R1
1K
R2
K1
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
50A
50B
51A
51B
PROG CKT
PROG CKT
OPROG1
OPROG2

FIG. 11